



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,957	10/24/2003	Anand Pande	14920US01	2011
23446 7590 07/23/2009 MCANDREWS HELD & MALLOY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661				
EXAMINER				
FRANKLIN, RICHARD B				
ART UNIT		PAPER NUMBER		
2181				
MAIL DATE		DELIVERY MODE		
07/23/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANAND PANDE

Appeal 2008-002572
Application 10/692,957
Technology Center 2100

Decided¹: July 23, 2009

Before JEAN R. HOMERE, JOHN A. JEFFERY, and
STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

¹ The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date.

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-19, 23, and 24. Claims 20-22 have been cancelled. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

The Invention

The disclosed invention relates generally to designing data structures including reducing a first Gray-code sequence into a second Gray-code sequence by removing pairs of mirrored Gray-codes from the first Gray-code sequence (Spec. 3.)

Independent claim 1 is illustrative:

1. An asynchronous first-in-first-out (FIFO) data structure, comprising:

a FIFO memory having a depth d in which d is an integer; and

a code generator coupled to the FIFO memory and providing a first code sequence of length $2d$, the first code sequence having a circular property and a Hamming length of one for any two consecutive codes of the first code sequence, the first code sequence being generated from a second code sequence by removing one or more pairs of mirrored codes of the second code sequence.

The References

The Examiner relies upon the following references as evidence in support of the rejections:

Pontius

US 6,337,893 B1

Jan. 08, 2002

Yi	US 6,703,950 B2	Mar. 09, 2004 (filed Sep. 14, 2001)
Miyamoto	US 6,810,468 B2	Oct. 26, 2004 (filed Dec. 04, 2001)

The Rejections

1. The Examiner rejects claims 1-4, 12, 13, 16, 23, and 24 under 35 U.S.C. § 103(a) as being unpatentable over Pontius and Yi.
2. The Examiner rejects claims 5-11, 14, 15, and 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Pontius, Yi, and Miyamoto.

ISSUE #1

Appellant asserts that “Pontius and Yi were improperly combined” (App. Br. 9) because “modifying the teachings of Pontius by the teachings of Yi leads to a modified invention in Pontius that is rendered unsatisfactory for its intended purpose” (*id.*).

Did Appellant demonstrate that the Examiner erred in finding that it would have been obvious to one of ordinary skill in the art to combine the Pontius and Yi disclosures in arriving at the claimed invention?

ISSUE #2

Appellant asserts that “the combination of Pontius and Miyamoto or the combination of Yi and Miyamoto cannot be maintained” (App. Br. 13) because “[t]he teachings of Pontius and Yi teach away from the teachings of Miyamoto” (*id.*).

Did Appellant demonstrate that the Examiner erred in finding that it would have been obvious to one of ordinary skill in the art to have combined the Pontius and Yi references with the Miyamoto reference in arriving at the claimed invention?

FINDINGS OF FACT

The following Findings of Facts (FF) are shown by a preponderance of the evidence.

1. Pontius discloses “a first-in-first-out (FIFO) device” and a “data unit is stored at a FIFO address indicated by a write pointer” (col. 1, ll. 27-31).
2. Pontius discloses that “[t]he counters are modulo in that they wrap to zero when a maximum count is reached” (col. 1, ll. 38-39).
3. Pontius discloses that “Gray codes can readily be constructed for any bit length” (col. 2, ll. 11-12) and that an “algorithm can be iterated to yield gray codes of any desired bit length” (col. 2, ll. 22-23).
4. Pontius discloses “an n-bit modulo-M gray-code counter in which the distribution of M gray-codes among $N=2^n$ possible n-bit gray codes has bilateral symmetry . . . [that is] translational, but it can also be reflective or both” (col. 3, ll. 11-15).
5. Pontius discloses that “[a] suitable gray code can be constructed for any selected modulo number that is divisible by four” (col. 3, ll. 21-22). In one example of Pontius, “[s]tart with a power-of-two gray

code for the next larger power of two . . . if $\frac{1}{2}N < M < N$, select the full n-bit modulo-N gray code. Then omit (skip) $(N-M)/4$ gray codes at the beginning of the modulo-N gray-code sequence, $(N-M)/2$ gray codes in the middle of the modulo-N gray-code sequence, and $(N-M)/4$ gray codes at the end of the modulo-N gray-code sequence. The result is a modulo-M gray code sequence” (col. 3, ll. 23-30).

6. Yi discloses that “iterative reflecting procedure for generating Gray code is known in the prior art” (col. 4, ll. 1-2).
7. Yi discloses in one example that “whenever an equal number of codes are removed from immediately above and below the axis of reflection of a Gray code sequence, the resulting sequence will always be Gray code” (col. 4, ll. 17-19).

PRINCIPLES OF LAW

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415 (2007).

ANALYSIS (ISSUE #1)

As set forth above, Pontius discloses data management in a FIFO system in using Gray codes and generating a gray code sequence (e.g., a modulo-M gray code sequence) by omitting pairs of mirrored codes from a “full n-bit modulo-N gray code” sequence (FF 1-5). Yi also discloses that iterative procedures for generating Gray code sequences “is known in the prior art” (FF 6, 7). We agree with the Examiner that it would have been obvious to one of ordinary skill in the art to have combined the Pontius and Yi disclosures as each of Pontius and Yi disclose that generating gray code sequences from other gray code sequences was known in the prior art.

Appellant argues that “Yi leads to a modified invention in Pontius that is rendered unsatisfactory for its intended purpose (e.g., simple detection of ‘full’ and ‘empty’ conditions when using read and write pointers with modulo numbers that are not powers of two)” (App. Br. 9). We disagree. Pontius explicitly discloses that a gray code sequence generated from a “full n-bit modulo-N gray code” sequence by omitting (mirrored) gray codes is applicable in the Pontius embodiments (FF 1-5). Yi confirms that such a “reflecting procedure . . . is known in the prior art” (FF 6). Thus, we find no indication, and Appellant has not indicated a logical rationale, that such a gray code sequence generated from a full-length gray code sequence as disclosed by Pontius would render the Pontius system unsatisfactory for its intended purpose. Indeed, such a conclusion would be counter-intuitive as it

would require a sequence generated by Pontius to be unsatisfactory for the Pontius system itself.

Appellant states that a specific example of Yi is “a method for generating a 4 bit modulo 12 grey code counter sequence for which there is no ‘simple detection of ‘full’ and ‘empty’ conditions when using read and write pointers with modulo numbers that are not powers of two’ [as in Pontius]” (App. Br. 9). However, Yi merely discloses the specific example “in order to highlight the symmetric architecture of Gray code” (col. 4, ll. 3-4) and to emphasize that reflecting procedures “for generating Gray code is known in the prior art” (col. 4, ll. 1-2). Indeed, Pontius discloses just such a procedure (FF 5). Appellant has failed to demonstrate that a specific example of Yi to demonstrate a property of Gray code sequences (i.e., “the symmetric architecture of Gray code”) somehow indicates that a Gray code sequence generated by Pontius is supposedly “unsatisfactory for its intended purpose” in the Pontius embodiment.

For at least the aforementioned reasons, we conclude that Appellant has not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner’s rejection of claims 1-19, 23, and 24 with respect to issue #1.

ANALYSIS (ISSUE #2)

The Examiner finds that “Pontius in combination with Yi does not teach that the code generator is coupled to a write pointer” (Ans. 7), but that

“Miyamoto teaches . . . a write pointer (Miyamoto; Figure 1 Item 21)” (*id.*). In addition, Pontius discloses a write pointer that indicates a FIFO address (FF 1). Because Pontius discloses a write pointer and Miyamoto further confirms that write pointers would have been known to one of ordinary skill in the art by disclosing a write pointer, we agree with the Examiner that it would have been obvious to one of ordinary skill in the art to have combined Pontius, Yi, and Miyamoto to at least obtain a gray-code counter system (Pontius) that includes a write pointer (Pontius and Miyamoto).

Appellant asserts that “Pontius disparages the 2^N depth FIFO of Miyamoto” (App. Br. 14). Even assuming Appellant’s contention to be true, we are unpersuaded by Appellant’s argument because Appellant has not demonstrated that Pontius also “disparages” utilizing a write pointer as demonstrated by Miyamoto. In fact, Pontius does utilize a write pointer which indicates that Pontius does not disparage such use.

For at least the aforementioned reasons, we conclude that Appellant has not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner’s rejection of claims 5-11, 14, 15, and 17-19 with respect to issue #2.

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that Appellant has failed to demonstrate that the Examiner erred in:

1. finding that it would have been obvious to one of ordinary skill in the art to combine the Pontius and Yi disclosures in arriving at the claimed invention (issue #1) and

2. finding that it would have been obvious to one of ordinary skill in the art to have combined the Pontius and Yi references with the Miyamoto reference in arriving at the claimed invention (issue #2).

DECISION

We affirm the Examiner's decision rejecting claims 1-19, 23, and 24 under 35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661